CLAIMS

What is claimed is:

1   1.   A content addressable memory (CAM) cell comprising:

2   four storage elements; and

3   four switching circuits each coupled between a first match line and a reference node, each

4   of the switching circuits having a first input coupled to a respective one of the four

5   storage elements, and a second input coupled to a respective one of four compare

6   lines.

1   2.   The CAM cell of claim 1 wherein, during a compare operation, the four switching circuits

2   receive a four-bit comparand value from the four compare lines, the four-bit comparand

3   value including three bits in a first state and one bit in a second state.

1   3.   The CAM cell of claim 1 wherein at least one of the switching circuits comprises first and

2   second transistors coupled in series between the first match line and the reference node, the

3   first and second transistors having respective control terminals that constitute the first input

4   and the second input of the at least one of the switching circuits.

1   4.   The CAM cell of claim 1 wherein the control terminals are gate terminals.

1   5.   The CAM cell of claim 1 wherein each of the switching circuits is a logic AND gate.

1   6.   The CAM cell of claim 1 further comprising four additional switching circuits each

2   coupled between a second match line and the reference node, and each having a first input

3   coupled to a respective one of the four storage elements, and a second input coupled to a

4   respective one of four additional compare lines.

1   7.   The CAM cell of claim 1 wherein the reference node is a ground reference node.

1   8.   The CAM cell of claim 1 wherein each of the storage elements is a static storage element.

1   9.   The CAM cell of claim 1 wherein each of the storage elements is a dynamic storage

2   element.

1   10.   The CAM cell of claim 1 wherein each of the storage elements is a nonvolatile storage

2   element.

1   11.   The CAM cell of claim 1 further comprising four pairs of access transistors, each pair of

2   access transistors being coupled between a respective one of the four storage elements and

3   a respective one of four pairs of bit lines.

1   12.   The CAM cell of claim 11 wherein the four pairs of access transistors each have a control

2   terminal coupled in common to a first word line.

1   13.   The CAM cell of claim 1 further comprising a first access transistor coupled between a first

2   one of the four storage elements and a first bit line, a second access transistor coupled

3   between the first one of the four storage elements and a second bit line, a third access

4   transistor coupled between a second one of the four storage elements and the first bit line,

5   and a fourth access transistor coupled between the second one of the four storage elements

6   and the second bit line.

1   14.   The CAM cell of claim 1 wherein the first and second access transistors have respective

2   control terminals coupled to a first word line, and the third and fourth access transistors

3   have respective control terminals coupled to a second word line.

1   15.   The CAM cell of claim 1 wherein the first input of each of the four switching circuits is

2   coupled to an inverting output of the respective one of the four storage elements.

1   16.   A content addressable memory (CAM) device comprising:

2   a plurality of columns of CAM cells; and

3   a plurality of decoder circuits to decode respective groups of bits of a comparand value into

4   corresponding sets of decoded signals, and coupled to provide each of the sets of

5   decoded signals to a respective one of the columns of CAM cells.

1   17.   The CAM device of claim 16 wherein each group of bits includes M constituent bits and

2   each corresponding set of decoded signals includes N constituent signals, N being greater

3   than M.

1   18.   The CAM device of claim 17 wherein $N = 2^M$.

1   19.   The CAM device of claim 16 wherein each of the groups of bits of the comparand value

2   includes two constituent bits and each corresponding set of decoded signals includes four

3   constituent signals.

1   20.   The CAM device of claim 16 wherein each of the plurality of decoder circuits decodes the

2   respective group of bits of the comparand value into the corresponding set of decoded

3   signals such that one signal of the set of decoded signals has a first state and the remaining

4   signals of the set of decoded signals have a second state.

1   21.   The CAM device of claim 20 wherein the one signal having the first state is a first, second,

2   third or fourth one of the decoded signals according to whether the corresponding group of

3   bits of the comparand value have a first, second, third or fourth state, respectively.

1   22.   The CAM device of claim 16 further comprising a plurality of mapping sub-circuits to

2   convert respective groups of bits of a write data value into corresponding sets of data state

3   signals, the mapping sub-circuits being coupled to provide the sets of data state signals to

4   the columns of CAM cells, respectively.

1   23.   The CAM device of claim 22 wherein the write data value comprises:

2   a data word having constituent data bits; and

3   a mask word having constituent mask bits, and wherein the each of the mapping sub-

4   circuits is configured to convert a respective group of the data bits and a respective

5   group of the mask bits into the corresponding set of data state signals.

1   24.   The CAM device of claim 22 wherein each of the sets of data state signals is a set of

2   complementary signals.

1   25.   The CAM device of claim 22 wherein each of the sets of data state signals includes N

2   signals in a first state and M minus N signals in a second state, N ranging from one to M

3   and being the number of permutations of a first group of bits of a comparand value that

4   match a corresponding one of the groups of bits of the write data value.

1   26.   The CAM device of claim 25 wherein the number of permutations of the first group of bits

2   of a comparand value that match the corresponding one of the groups of bits of the write

3   data value is one (1) if no mask bits included within the corresponding one of the groups of

4   bits of the write data value indicate a mask condition.

1   27. The CAM device of claim 25 wherein the number of permutations of the first group of bits

2   of a comparand value that match the corresponding one of the groups of bits of the write

3   data value is 2^R, R being the number of mask bits included within the corresponding one of

4   the groups of bits of the write data value that indicate a mask condition.

1   28. A content addressable memory (CAM) device comprising:

2   an array of CAM cells;

3   a write mapping circuit to convert an input data word into a converted data word having

4   one of at least two different patterns of constituent bits according to the state of a first

5   control signal; and

6   a read/write circuit coupled to receive the converted data word from the write mapping

7   circuit and coupled to the array of CAM cells to output the converted data word

8   thereto.

1   29. The CAM device of claim 28 wherein the two different patterns of bits comprise equal

2   numbers of bits.

1   30. The CAM device of claim 28 wherein the input data word includes data bits and mask bits

2   with each of the data bits and mask bits constituting a respective data/mask bit pair, and

3   wherein each set of four bits within the converted data word includes 2^R bits in a first state

4   and the remaining bits in a second state if the first control signal selects a first conversion

5   mode, R being the number of mask bits in a masking state within a group of two data/mask

6   bit pairs.

1   31.   The CAM device of claim 30 wherein each set of four bits within the converted data word

2   includes R-2 bits in a first state and the remaining bits in a second state if the first control

3   signal selects a second conversion mode.

1   32.   The CAM device of claim 31 wherein the converted data word is complemented prior to

2   being stored within the array of CAM cells if the first control signal selects the second

3   conversion mode.

1   33.   The CAM device of claim 30 wherein the converted data word is complemented prior to

2   being stored within the array of CAM cells if the first control signal selects the first

3   conversion mode.

1   34.   The CAM device of claim 28 further comprising a write data selector having a first input

2   port coupled to receive the converted data word from the write mapping circuit and a

3   second input port coupled to receive the input data word, the write data selector being

4   responsive to a second control signal to output either the converted data word or the input

5   data word to the read/write circuit.

1   35.   The CAM device of claim 28 further comprising a read mapping circuit coupled to receive

2   a read data word from the read/write circuit and configured to convert the read data word

3   into a converted data word having one of at least two different patterns of constituent bits

4   according to the state of the first control signal.

1   36.   A method of operation within a content addressable memory (CAM) device, the method

2   comprising:

3   decoding respective pairs of bits within a comparand value into corresponding four-bit map

4   values in which one bit is in a first state and the remaining three bits are in a second

5   state; and

6   outputting each of the map values onto a respective set of four compare lines within the

7   CAM device.

1   37.   The method of claim 36 further comprising storing the comparand value in a comparand

2   register prior to decoding the respective pairs of bits.

1   38.   The method of claim 36 further comprising storing the map values in a comparand register

2   prior to outputting the map values onto respective sets of compare lines.

1   39.   The method of claim 36 further comprising selecting either a first operating mode or a

2   second operating mode within the CAM device, and wherein decoding respective pairs of

3   bits within a comparand value into corresponding four-bit map values comprises decoding

4   the respective pairs of bits within the comparand value into corresponding four-bit map

5   values if the first operating mode is selected.

1   40.   The method of claim 39 further comprising outputting each bit of the comparand value in

2   complementary form onto a respective pair of the compare lines within the CAM device if

3   the second operating mode is selected.

1   41.   A method of operation within a content addressable memory (CAM) device, the method

2   comprising:

3   receiving an N-bit comparand value; and

4   activating less than N compare lines within the CAM device to compare each of the N bits

5   of the comparand value with contents of CAM cells coupled to the N compare lines.

1   42.   The method of claim 41 further comprising converting the N-bit comparand value into a

2   2N-bit compare word in which each group of four bits includes one bit in a first state and

3   three bits in a second state.

1   43.   The method of claim 42 wherein activating less than N compare lines within the CAM

2   device comprises activating a selected compare line within each set of four compare lines,

3   the selected compare line corresponding to the one bit in the first state.

1   44.   The CAM device of claim 43 wherein activating the selected compare line comprises

2   outputting a logic high signal on the selected compare line.

1   45.   The method of claim 42 wherein converting the N-bit comparand value into a 2N-bit

2   compare word comprises decoding each pair of bits in the comparand value into respective

3   groups of four bits in which each group of four bits includes the one bit in the first state and

4   the three bits in the second state.

1   46.   The method of claim 41 further comprising:

2   receiving a 2N-bit write value containing N data bits and N mask bits, each of the mask bits

3   corresponding to a respective one of the data bits to form a data/mask pair; and

4   converting each distinct group of four bits within the write value into a corresponding four-

5   bit map value having 2^R bits in a first state and remaining bits in a second state, R

6   being the number of mask bits in the distinct group of four bits within the write value

7   that are in a masking state.

1 47. The method of claim 46 wherein each distinct group of four bits within the write value

2   includes two mask bits and two data bits.

1 48. The method of claim 46 further comprising outputting the map value onto a set of bit lines

2   for storage within a CAM cell within the CAM array.

1 49. A method of operation within a content addressable memory (CAM) device, the method

2   comprising:

3   converting a four-bit write data entity containing two mask bits and two data bits into a

4   four-bit data map value having 2^R bits in a first state, R being the number of mask bits

5   in the write data entity that indicate a masking condition; and

6   providing a complement of the data map value to a compare circuit within a CAM cell.

1 50. The method of claim 49 further comprising:

2   converting a two-bit comparand entity into a four-bit comparand map value having one bit

3   in the first state and remaining bits in a second state; and

4   providing the comparand map value to the compare circuit.

1 51. The method of claim 50 further comprising comparing the comparand map value with the

2   complement of the data map value within the compare circuit.

1 52. The method of claim 51 wherein comparing the comparand map value with the

2   complement of the data map value comprises providing the four-bits of the complement of

3   the data map value to first inputs of respective switching circuits within the compare circuit

4   and providing the four-bits of the comparand map value to second inputs of the respective

5   switching circuits.

1   53.   The method of claim 52 wherein each of the switching circuits within the compare circuit

2   is switched to a conducting state if the bits of the complement of the data map value and

3   the comparand map value are both in the first state.

1   54.   The method of claim 52 wherein each of the switching circuits are coupled between a first

2   match line and a reference node.

1   55.   A content addressable memory (CAM) device comprising:

2   a CAM array having a plurality of columns of CAM cells;

3   means for decoding respective pairs of bits within a comparand value into corresponding

4   four-bit map values in which one bit is in a first state and the remaining three bits are

5   in a second state; and

6   means for outputting each of the map values to a respective one of the columns of the

7   CAM cells.

1   56.   A content addressable memory (CAM) device comprising:

2   a CAM array having a plurality of CAM cells and 2N compare lines, N being an integer

3   value;

4   means for receiving an N-bit comparand value; and

5   means for activating less than N of the 2N compare lines within the CAM device to

6   compare each of the N bits of the comparand value with contents of CAM cells

7   coupled to the 2N compare lines.

1   57.   The CAM device of claim 56 further comprising means for converting the N-bit

2   comparand value into a 2N-bit compare word in which each group of four bits includes one

3   bit in a first state and three bits in a second state.

1   58.   The CAM device of claim 57 wherein activating less than N of the 2N compare lines

2   comprises means for activating a selected compare line within each set of four compare

3   lines, the selected compare line corresponding to the one bit in the first state.

1   59.   A content addressable memory (CAM) device comprising:

2   a CAM cell including a storage circuit and a compare circuit;

3   means for converting a four-bit write data entity containing two mask bits and two data bits

4   into a four-bit data map value having 2^R bits in a first state, R being the number of

5   mask bits in the write data entity that indicate a masking condition; and

6   means for providing a complement of the data map value to the compare circuit.

1   60.   The CAM device of claim 59 further comprising:

2   means for complementing the data map value to generate the complement of the data map

3   value; and

4   means for storing the complement of the data map value in the storage circuit.

1   61.   The CAM device of claim 59 further comprising means for storing the data map value in

2   the storage circuit, and wherein the storage circuit comprises means for providing the

3   complement of the data map value to the compare circuit.